VLSI ARRAY PROCESSOR

R & D STATUS REPORT

DARPA ORDER NO. 4001

CONTRACT NO. N00014-80-C-0693

CONTRACT DATE: August 1, 1980

PRINCIPAL INVESTIGATOR: Ed Greenwood

PHONE: (602)949-3394

November 19, 1982

REPORTING PERIOD - June 30, 1982 thru November 15, 1982

APPROVED BY: _____

Bob Pfeifer
Section Manager
Secure Processor Systems

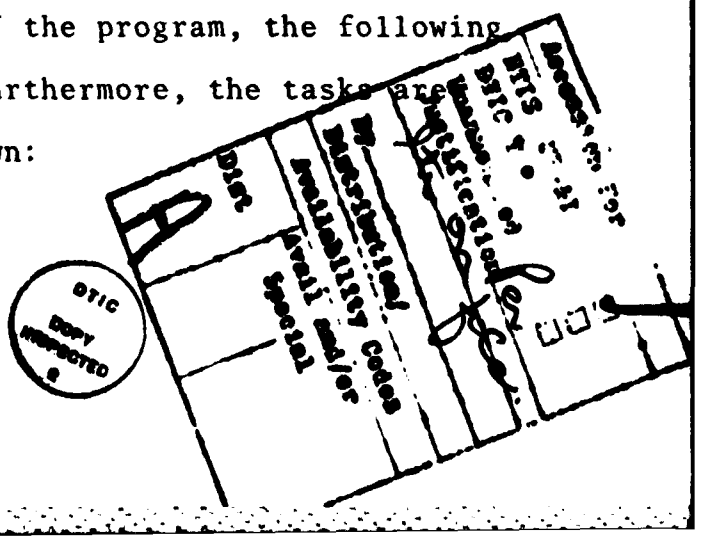
The first lot (10 wafers per lot) of the Arithmetic Processor Units (APU) are 90% of the way through the fabrication cycle. Eight (8) good wafers out of the ten (10) original wafers look good by visual inspection. The eight wafers have successfully completed the platinum silicide deposition; which visually looks good on the eight wafers.

Since the end of October, miscellaneous problems have occurred with the mask stepper equipment. As a result, we have virtually stopped processing APU devices until reliable operation of the stepper is obtained. Parts have been ordered and work is underway to correct the problem. Reliable operation is expected to be restored by the first week of December.

Two other lots, that were less than 50% through the fabrication cycle were lost due to operator errors. A fourth lot has been started and is 10% of the way through the fabrication cycle.

CHI completed the integration and test of the APU breadboard in September and October. The integration used one of the demo systems (with its associated modules) to verify APU breadboard operation. The APU breadboard has been delivered to Motorola. The APU chip test software will be verified using the APU breadboard in conjunction with the chip/wafer test system. This testing has just been initiated.

With the impending culmination of the program, the following tasks are proposed for completion. Furthermore, the tasks are ranked in order of importance, as shown:



1. APU chip fabrication and verification

2. Integration and checkout of APU chip in demonstration system

3. Demonstration system interoperation with Lincoln Lab terminal

4. APU chip microcode assembler and simulator

5. Demonstration system macro assembler

6. Demonstration system microcode assembler

7. Demonstration system microcode simulator

Of the above items, numbers 4, 5, and 6 have been completed. Until items 1 and 2 are completed, no more effort is being expended on items 3 and 7. However, at this time we expect to complete all of the above items.

The following activities are planned for the rest of November and December.

1. Complete fabrication of the first lot of APU devices

2. Verify LSI APU tests with the APU breadboard

No technical problems are foreseen at this time. A funds expenditure report is attached.

Date Prepared October 13, 1982
Contract No. N00014-80-C-0693
Contractor Motorola Inc. GEG

FUNDS EXPENDITURE REPORT

Summary Work Package Title Array Process
Report Month September 1982

Column A ORIGINAL PROPOSAL	Column B Latest Accepted Revised Proposals (if any)	Column C Reporting Month Expenditures	Column D Cumulative Expenditures To Date			Column E Cost Complete estimate **	Column F Latest Cost Estimate (D2 plus E) **
			D1 Total Man Hours	D2 Dollar Value	D3* Percentage Dollar Value		
1. DIRECT LABOR							
Type No. of Hours@ Hourly Rate Dollar Total							
Total Direct Labor 161363	246014	4102	14542	221733	90.1	24281	246014
Overhead 155230	229245	3652		210205	91.7	19040	229245
Total direct labor & O'Head 316593	475259	7754		431938	90.9	43321	475259
2. MATERIALS & PARTS 500256	524842	6784		430145	82.0	94697	524842
3. TRAVEL EXPENSE 20120	19032	305		11160	58.6	7872	19032
4. COST OF MONEY 9900	33225	558		28158	84.7	5067	33225
5. GEN & ADMN 156938	203775	6876		173569	85.2	30206	203775
6. OTHER COSTS 86193	98867	1167		80684	81.6	18183	98867
TOTAL COSTS 1090000	1355000	23444		1155654	85.3	199346	1355000
7. FIXED FEE (OR PROFIT) 99000	99000	127		98050	99.0	950	99000
TOTAL CONTRACT PRICE 1189000	1454000	23571		1253704	86.2	200296	1454000
***OUTSTANDING COMMITMENTS -	-	-		116702	-	(116702)	-
TOTAL COMMITMENTS AND EXPENDITURES 1189000	1454000	23571		1370406	94.2	83594	1454000

O/S MAT'L
OTHER